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MAINS POWER QUALITY THD ANALYZER

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Abstract
This paper presents the design and development of a Mains Power Quality THD Meter, a dedicated device designed for real-time monitoring of total harmonic distortion (THD) in the electrical grid. As modern power systems face increasing degradation due to non-linear loads, continuous tracking of power quality parameters has become essential. The developed system measures voltage signals and frequency directly from the mains supply, processes the data using STM32H750VBT6 microcontroller, and displays the calculated THD values on a conveniently designed GUI of the PC and the TFT display. Experimental results demonstrate that the device provides accurate, reliable, and cost-effective monitoring, making it a practical tool for assessing power quality in both residential and laboratory environments.

Keywords: Total Harmonic Distortion (THD), Power Quality Monitoring, STM32H750, Real-Time FFT, Non-linear Loads, Dual-Channel Simultaneous Sampling, Graphical User Interface (GUI).

INTRODUCTION

The global proliferation of power electronics and switch-mode power supplies (SMPS) has fundamentally transformed the landscape of modern low-voltage electrical distribution networks. While these technologies offer unparalleled energy efficiency and precise control for consumer electronics, industrial drives, and household appliances, they inherently introduce a significant drawback to the grid: non-linear current consumption. Devices such as computers, LED lighting, variable-frequency drives, and domestic heating appliances draw current in short, abrupt pulses rather than a continuous sinusoidal waveform. This cumulative non-linear behavior distorts the current wave shape across the network, which subsequently induces harmonic voltage distortion across the network impedance, leading to a severe degradation of the overall Mains Power Quality (MPQ).

Voltage harmonic distortions are highly detrimental to electrical infrastructure and connected equipment. The presence of higher-order voltage harmonics (typically up to the 40th harmonic in standard compliance testing) induces parasitic core losses and excessive overheating in distribution transformers, accelerates the degradation of insulation materials, and causes premature aging of power factor correction capacitors. Furthermore, localized voltage waveform distortion can cause malfunctions in sensitive laboratory instruments, trigger false trippings of protective relays, and inject audible noise into communication lines. Consequently, real-time tracking, mitigation, and high-fidelity measurement of Total Harmonic Distortion (THD) in the voltage domain have shifted from being an intermittent maintenance requirement to a critical continuous monitoring necessity for both industrial facilities and smart-grid residential nodes.

Traditional power quality analyzers capable of precise voltage harmonic profiling utilize high-end, multi-channel data acquisition systems coupled with complex digital signal processors [1]. While these

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instruments offer laboratory-grade accuracy, their restrictive cost and bulky form factors make widespread, decentralized deployment economically unfeasible. Conversely, commercial low-cost smart meters often lack the computational bandwidth required to perform continuous, high-resolution spectral decomposition of the voltage waveform, typically relying on simplified root-mean-square (RMS) approximations that fail to capture transient harmonic anomalies or high-frequency switching noise superimposed on the fundamental grid frequency.

To bridge this gap, this paper introduces a low-cost, high-performance, edge-computing Mains Power Quality THD Analyzer built upon the advanced ARM Cortex-M7 architecture. By leveraging the specific hardware peripherals of the STM32H750VBT6 MCU [2] - specifically its regular analog-to-digital conversion (ADC) and high-speed Direct Memory Access (DMA) controllers - the proposed system achieves deterministic high-fidelity sampling of the mains voltage channel at a precise sampling rate of 12.8 kHz. This hardware-driven sampling approach ensures absolute temporal precision, completely eliminating timing jitter which is a notorious bottleneck in purely software-triggered data acquisition topologies.

The onboard firmware handles real-time execution of the CMSIS-DSP library [2], performing 512-point Fast Fourier Transforms (FFT) on windowed voltage sample blocks. This edge-computed harmonic spectrum is then packaged into high-density telemetry streams and transmitted via a Virtual COM Port (VCP) over a native USB User Device interface to a custom Python-based graphical user interface (GUI). The resulting system delivers a compact, cost-effective, and standalone laboratory grade instrumentation platform capable of visualizing stable grid waveforms, tracking mains frequency down to two decimal places, and performing real-time spectral decomposition of grid voltage anomalies.

HARDWARE ARCHITECTURE AND SIGNAL CONDITIONING

The analog front-end of the analyzer is designed around a custom-modified ZMPT101B voltage transformer module to safely step down the 230V RMS mains supply and shape the waveform for digital acquisition. The isolated voltage transformer features a 1:1 turns ratio with exactly 1000 turns on both the primary and secondary windings. By operating strictly within its linear core characteristic, the transformer is guaranteed to avoid magnetic saturation limits, ensuring high-fidelity harmonic reproduction [5].

To restrict the primary winding current to a safe micro-current level, a high-value current-limiting resistor of 820k is connected in series with the primary input. The secondary winding is terminated across a 100Ohm load resistor, which converts the isolated current loop back into a proportional small-signal AC voltage. This low-amplitude AC signal is routed directly to the first stage of an on-board active operational amplifier network, configured as a non-inverting amplifier with a voltage gain of 10. This first stage also injects a DC offset component equal to Vdd/2.

Following the initial amplification, the signal passes through a trimming potentiometer circuit. This component attenuates the waveform amplitude while intentionally eliminating the initial DC bias component. The decoupled AC signal is then fed into the second amplification stage, which consists of another non-inverting operational amplifier configuration with a voltage gain of 10.

Because the physical signal conditioning module is powered from a stable 5V, a standard symmetrical voltage divider would inherently establish a 2.5V DC bias level. Since a 2.5 V bias is incompatible with the 3.3 V full-scale input requirements of the microcontroller, one of the two biasing

resistors in the second-stage potential divider network was physically modified. This hardware modification successfully shifts the injected DC offset component down to exactly 1.65V (corresponding to the ideal Vdd/2 of a 3.3 V system).

Figure 1 shows the simple hardware of the THD analyzer contained modified ZMPT101B module and FK750M1 board.

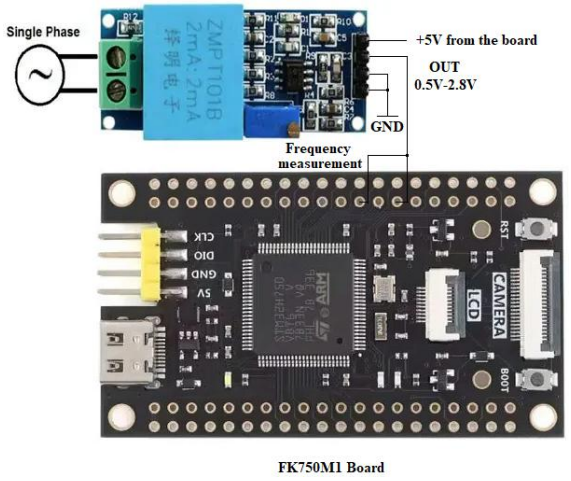


Fig. 1. *The hardware of the THD analyzer.*

As can be seen in Fig. 1, the conditioned single-ended voltage waveform, centered on the 1.65V DC baseline, is routed directly from the active conditioning network to the physical input pin of A/D1 converter, channel 3 (mapped to microcontroller pin PA6) [2]. Due to the precise combination of the series current-limiting network, load termination, dual-stage amplification gains, and fine-tuning via the trimming potentiometer, the dynamic voltage swing at the A/D input is tightly bounded between 0.5V and 2.8V under nominal grid conditions. Also, pin PA6 (A/D input) is shorted with the noninverted input of the analog comparator COMP1 (PB0 pin) whose out triggers the TIM1 in input capture mode. This part of the system was used for accurate frequency measurement.

Mentioned optimized voltage window offers significant engineering advantages for high-fidelity harmonic profiling:

a) *Saturation Prevention*: By restricting the peak-to-peak voltage swing from exceeding the 0 V ground floor and the 3.3 V power rail, the analog signal is strictly protected from clipping distortions, enabling the analyzer to capture high-order voltage harmonics without waveform flat-topping.

b) *Linearity Optimization*: Operating the internal ADC input stage away from the extreme boundaries of its unipolar range eliminates the non-linear errors typically induced by the microcontroller's sampling switches near the rail limits.

c) *Transient Headroom*: Keeping the normal grid peaks at 2.8 V provides a safe, non-saturating headroom up to 3.3 V, allowing the device to linearly capture transient over-voltage anomalies and high-amplitude harmonic surges superimposed on the mains supply.

FIRMWARE ARCHITECTURE AND DIGITAL SIGNAL PROCESSING

The deterministic tracking and real-time execution of the grid monitoring mathematical loops are performed entirely within the 32-bit ARM Cortex-M7 digital signal processing core of the high-performance STM32H750VBT6 MCU.

To establish a rigid and precise temporal foundation for spectral calculations, software-based polling loops and regular conversion interrupts are completely avoided. Instead, data acquisition is driven entirely by an internal hardware master timer (TIM2) running a precise update frequency of 12800Hz [2]. Each hardware update trigger commands ADC1 to perform an instant analog-to-digital conversion loop. This sampling interval captures exactly 256 discrete samples per single 20ms utility grid cycle, ensuring full compliance with compliance testing up to the 40th harmonic component without any timing drift.

The captured 16-bit unipolar samples are immediately offloaded from the peripheral register by DMA1 stream 0, configured in continuous circular mode [2]. The DMA stream manages a large double-buffered array in the internal SRAM domain, utilizing hardware half-transfer and transfer-complete interrupt flags to pass

ready data blocks to the processing thread while the peripheral continuously populates the alternative memory block. This direct-to-memory hardware routing guarantees zero CPU overhead during the high-speed data acquisition phase, leaving the full computational bandwidth of the processor available for the real-time Fourier transform execution.

REAL TIME SPECTRAL DECOMPOSITION AND VOLTAGE THD COMPUTATION

Once the fresh sample block of 512 real samples is fetched into the digital processing segment, the local DC bias offset injected by the analog operational amplifier is calculated and subtracted numerically to yield a clean, zero-centered AC waveform. To prevent spectral leakage faults caused by non-integer cycle sampling and window boundaries truncation, the raw zero-centered voltage array is multiplied element-by-element with a pre-computed Hanning window vector [4].

The windowed signal is passed immediately into the high-performance ARM CMSIS-DSP library routines [2]. The embedded application executes a 512-point real Fast Fourier Transform (RFFT) followed by a fast complex magnitude block:

```
arm_rfft_fast_f32(&fft_handler, fft_input,
fft_output, 0);

arm_cmplx_mag_f32(fft_output,
magnitudes, FFT_SIZE / 2);
```

The fundamental grid component V_1 is localized precisely at spectral bin index 2, corresponding to the 50Hz grid frequency. The application then runs a fast localized summation loop to calculate the squared magnitudes of the higher-order spectral components up to the 40th harmonic order (bin index 80 - 2000 Hz) [2]

$$Harmonic_sum = \sum_{h=2}^{40} (M_h)^2 \qquad (1)$$

where M_h represents the complex magnitude extracted from the h-th harmonic bin. Finally, the total harmonic distortion (THD) of the mains voltage signal is computed as the ratio of the root-sum-square of the individual harmonic components to the fundamental amplitude, expressed as a precise percentage:

$$THD_{voltage} = \frac{\sqrt{Harmonic_sum}}{V_1} 100 \qquad (2)$$

This edge-calculated THD value, the exact fundamental grid frequency tracked via input capture of the timer TIM1, and the raw 256-point voltage wave cycle are packaged into optimized telemetry streams and transmitted via a USB Virtual COM Port (VCP) to the PC client.

PC CLIENT AND GRAPHICAL USER INTERFACE DESIGN

The desktop visualization layer and data logging interface are implemented within a highly responsive, custom-engineered Python application. This client-side platform establishes a real-time connection with the microcontroller via a virtual serial communication node over the native USB CDC drajver infrastructure.

To prevent visual stuttering and guarantee deterministic rendering frames, the software structure isolates the raw data reception loop from the main application thread. A non-blocking background worker continuously captures incoming serial bytes from the OS buffer and appends them to a unified dynamic string array. The system evaluates the incoming string for an explicit text line marker in the form of
marker = "----------"
Upon marker detection, a customized telemetry parser uses compiled regular expression (Regex) expressions to extract the edge-computed RMS voltage, peak amplitude voltage V_{max}, tracked grid frequency, and overall spectral THD. Simultaneously, the parser extracts the raw, high-density wave array bounded by the WAVE: indicator.

The extracted telemetry data is routed directly to a dual-panel visualization GUI built upon the high-performance Matplotlib animation framework. The layout is optimized into a specific split configuration, see Fig 2:

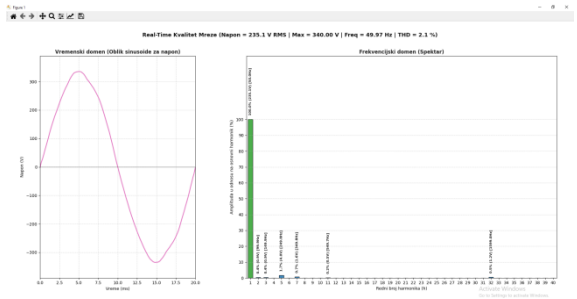


Fig. 2. *Dual panel, real-time visualization GUI.*

Left Panel (Time-Domain Oscilloscope): This sub-plot handles the geometric reconstruction of the utility grid cycle. Although the incoming text array carries 256 discrete points of the raw cycle, standard digital visualization requires an absolute circular closure to prevent the waveform endpoints from drifting or clipping on the screen. To achieve perfect boundary alignment, the application copies the initial sample (index 0) and appends it to the very end of the memory array, expanding the plot vector to exactly 257 points. This array is filtered through a low-pass 5-point moving average convolution window to suppress localized high-frequency digitizing noise without affecting phase parameters. The resulting curve starts and ends symmetrically, showing a clean 20.0ms period.

Right Panel (Frequency-Domain Spectrum): This sub-plot displays a live, dynamic bar chart of the individual voltage spectral harmonics from the 2nd up to the 40th order. Each vertical bar dynamically scales in amplitude relative to the fundamental 50Hz component (defined as 100%). The bar chart updates in exact synchronization with the oscilloscope display every 100ms, giving the operator an instantaneous visual signature of the electrical network's quality.

EXPERIMENTAL RESULTS

The analytical accuracy and operational stability of the developed analyzer were evaluated by continuously monitoring a standard low-voltage residential grid node. As can be seen on the Fig. 2, under nighting operating conditions of the grid, the system recorded a highly consistent and stable telemetry stream with a root-mean-square voltage of 235.1V, a peak amplitude of 340.0V, and a tracked grid frequency of 49.97Hz. The time-domain oscilloscope panel on the PC client reconstructed the grid cycle with high geometric fidelity, demonstrating an absolute boundary closure where the waveform begins at 0.0 ms, executes a precise median zero-crossing at 10.0 ms, and converges back onto the zero baseline at exactly 20.0ms without any endpoint drifting.

The frequency-domain panel registered an exceptionally clean voltage profile with an overall calculated THD of 2.1%, which complies with the rigorous limits defined by international standards (EN50160). Spectral decomposition confirmed that the distortion is predominantly driven by low-order odd components (3rd, 5th, and 7th harmonics), caused by non-linear domestic switch-mode loads circulating through the network impedance. At a clock frequency of 480 MHz, the ARM Cortex-M7 core executed the 512-point real FFT loops, Hanning window multiplications [4], and input capture tracking within a fraction of a millisecond. This deterministic edge-processing eliminated data-packet drops and timing jitter [3], verifying the long-term reliability of the system as a cost-effective, laboratory-grade instrumentation platform.

CONCLUSION

This paper has presented the design and laboratory validation of a compact, high-performance, and cost-effective Mains Power Quality THD Analyzer utilizing the advanced STM32H750VBT6 MCU. By leveraging a high-fidelity hardware data acquisition layer operating at a deterministic sampling rate of 12800Hz and

executing optimized ARM CMSIS-DSP real-time Fourier transform routines, the embedded platform achieves laboratory-grade tracking of grid voltage dynamics and spectral distortion signatures. Experimental results under real grid environments demonstrate stable frequency tracking at about 50.0Hz and highly accurate voltage THD logging from 2.1% to 2.4%**,** conforming fully to the strict compliance metrics enforced by international grid standards. The seamless virtual communication link and synchronized Python-based GUI ensure continuous, non-blocking telemetry visualization without packet drops. The resulting architecture delivers a robust, standalone tool uniquely suited for decentralized power quality assessment in both residential smart-grid nodes and academic research laboratories.

Further improvement of the proposed THD analyzer's functionality will be focused on the current spectrum of the individual consumers.

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