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IMPACT OF THE LEESON FREQUENCY–TO–PLL BANDWIDTH RATIO ON PHASE NOISE IN FREQUENCY SYNTHESIZERS

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Abstract
In hybrid DDS based PLL synthesizer, the phase noise is related to the interaction between the VCO Leeson frequency f_L and the PLL bandwidth F_{BW}. This interaction can be represented by $k = f_L/F_{BW}$, where f_L and F_{BW} are respectively, the Leeson frequency of the VCO and the bandwidth of the PLL within a composite hybrid noise model. The free running VCO model was found to match similarly results obtained from the measurement of a MAX2605 oscillator model by PN2060C, while the closed loop system was studied numerically. A Monte Carlo simulation of 3500 randomly generated configurations, subject to the imposed constraint of $F_{BW} \leq f_{PFD}/3$ had a 49.7% occurrence of reaching the imposed bandwidth limit. In all other 1762 configurations that simulated a true minimum jitter, the median was 1.25 and the 5–95% range 0.55–1.75. So, k is a helpful indicator of the trade-off, but the best k will be determined by the overall composite spectrum, and whether the bandwidth is bounded or not.

Keywords: phase noise (PN), PLL, DDS, Leeson frequency, loop bandwidth, VCO.

INTRODUCTION

The ratio $k = f_L/F_{BW}$, which is the voltage-controlled oscillator (VCO) Leeson frequency divided by phase locked loop (PLL) bandwidth is defined and evaluated in a composite hybrid synthesizer phase-noise model; several noise contributing blocks whose phase-noise effects are shaped by the closed-loop transfer function of the PLL are combined to form the PLL frequency synthesizer. A VCO with MAX2605 circuit is experimentally characterized and a closed loop is investigated numerically. To investigate this trade-off, a Monte Carlo analysis was performed on 3500 randomly generated combinations of reference, PLL and loop filter. In some configurations the jitter has an interior minimum, while in others the optimum is at the imposed bandwidth limit.

EXPOSITION

I. Architecture and Building Blocks of Hybrid PLL Frequency Synthesizers

The detailed treatment of the core architecture of a classical charge-pump PLL with phase-frequency detector (PFD), Loop Filter, VCO and feedback frequency divider is presented in [1]. In the studied case, the PFD, CP and digital control logic are implemented using one IC and the VCO is an external discrete module. A programmable R-divider is placed at the reference input of the PFD. It sets the comparison frequency, i.e. the rate at which the PFD compares the phase and frequency of the reference signal with those of the divided VCO output – Fig. 1.

The loaded quality factor Q_L and close-in phase noise are determined by quality factor Q_I of the tank inductor. A key relationship considered in this paper is the relationship between the VCO's Leeson frequency f_L and the loop bandwidth, which is a free design parameter but can be adjusted in relation to f_L to minimize total output phase noise.

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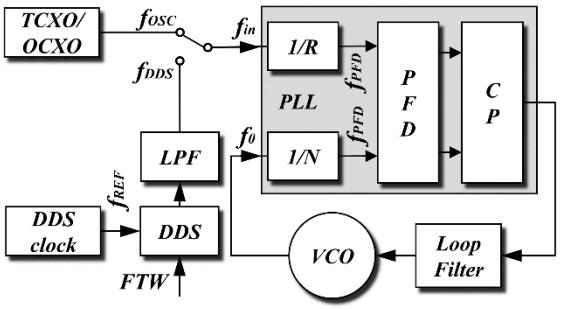


Fig. 1. *Architecture of hybrid synthesizer*

As the reference source, this work adopts a Direct Digital Synthesizer (DDS) rather than a simple crystal oscillator, for the fine frequency resolution and tuning agility multi-band operation requires – at the cost of its own phase-noise contribution. Because realistic DDS output spectra cannot be achieved through an ideal clock scaling, the residual-noise model from [2] is used as the reference-path input signal to the composite PLL-noise model provided in this work.

II. VCO PN Characterization: The Leeson Model and Types of Spectral Behavior

Many different phase-noise models have been developed [3] and Leeson is chosen because it does not require any access to the transistor level details of the circuit, which would not be possible for a packaged VCO. Two characteristic frequencies can be identified and they determine the shape of $S_\phi(f)$ [3]. The corner frequency f_c is the frequency at which the $1/f$ flicker-noise contribution crosses the white-noise floor, and the Leeson frequency f_L is:

$$f_L = \frac{1}{2\pi\tau} = \frac{f_0}{2Q_L}, \qquad (1)$$

where τ is the resonator relaxation time and Q_L is its loaded quality factor. If the loop is operated below f_L, the oscillator integrates the phase fluctuations of the amplifier, and their power spectrum is multiplied by approximately $\left(\frac{f_L}{f}\right)^2$ – the Leeson effect [3]. The framework is still used as a benchmark for today's silicon-based oscillators [4].

The relative order of f_c and f_L defines two types of spectral behavior [4]. Type 1 ($f_c < f_L$) is characteristic of low-Q_L resonators, where the Leeson effect applies to the white noise, giving the $1/f^3$, $1/f^2$ and f^0 regions. Type 2 ($f_L < f_c$) is characteristic of high-Q_L quartz or FBAR resonators, in which the spectrum passes from the $1/f^3$ region directly to the $1/f$ region, without an extended $1/f^2$ interval.

Type 1 are the most practical VCOs, in which the loaded Q_L is much lower than the Q of quartz/FBAR oscillators, be it external or internal. The PLL loop bandwidth is freely adjustable and can be placed in relation to f_L (e.g. below or above f_L to optimize composite phase noise) even with a manufacturer set inductor. The above is representative of type 2 behavior found in high-Q quartz/FBAR resonators, which are narrowband devices and for which the DDS-driven topology of interest in this study is not applicable; they come into play when the output frequency of the synthesizer is constant or capable of changing over a relatively small bandwidth.

The analysis is therefore limited to Type 1, which is used by VCOs based on the MC1648 to integrated products like the MAX2620 and MAX260x family.

III. Loaded Q-Factor (Q_L) Determination

For a Type 1 oscillator, the three characteristic slopes (-30 dB/dec, -20 dB/dec and 0 dB/dec) of the phase noise spectrum $S_\phi(f)$ locate the $1/f^3 - 1/f^2$ intersection at f_c and the $1/f^2$– white-noise boundary at f_L; Q_L is then determined using Eq. (1) with the known carrier frequency f_0. The procedure can be applied to any type 1 VCO, external and integrated inductor, and it only needs the measurable PSD curve and f_0.

Manufacturer datasheets provide a quick first order estimate for a specific situation under a specific inductor/inductive condition and a specific bias assumption, but they do not provide the actual Q_L that is measured in the study circuit and are correct only if the $Q_I - Q_L$ relationship is verified by direct measurement with a phase noise analyzer.

In this work both are used together: Data sheet values are used for a startup reference, and verify by direct measurement on a VCO

module.

IV. PLL Loop Bandwidth and Loop Filter Design Considerations

The charge pump current pulses are converted into the VCO tuning voltage by the loop filter. The transfer function $G(s)$ is determined by the impedance $Z(s)$ and the gains K_{PD}, K_{VCO} and divider ratio N of the PFD and the VCO. A passive (2nd/4th order) realisation of $Z(s)$ is used unless the required tuning-voltage swing is beyond the range that the charge-pump can deliver. If the order of the filter is fixed, its time constants are determined from the other filter design parameters, which are the loop bandwidth, the phase margin (30° to 80° [5] is common), the gamma optimization factor, and two pole ratios [6] which represent a compromise between closed-loop peaking and roll-off sharpness and between spur suppression.

This trade-off also has an impact on link margin and radio coverage in general, such as in LoRaWAN/IoT network surveys [7]. Of the five design degrees of freedom, only the loop bandwidth enters the composite noise model: the partitioning of the output spectrum between reference-path-dominated and VCO-dominated regions is set by the ratio f_L/F_{BW}, irrespective of the particular loop-filter realisation.

The loop bandwidth, F_{BW} (or $\omega_{BW} = 2\pi F_{BW}$) is the frequency at which the normalised loop gain is one. It is the dividing line between the two regimes of the closed loop: If the frequency f is below the frequency F_{BW}, the loop gain is greater than unity and the free-running VCO phase noise is suppressed, and the output is essentially the sum of the contributions from the reference and PFD/CP; if the frequency f is above the frequency F_{BW}, the loop gain is less than unity, and the output approaches the free-running VCO spectrum [6]. The natural starting value BW_{JIT} of F_{BW} [6] is then the offset at which the in-band reference/PFD/CP contribution crosses the free running VCO phase-noise PSD.

V. Composite Phase Noise Model: The Role of the f_L/F_{BW} Ratio

The DDS/reference path, PFD/CP block and free running VCO are connected to the output via different transfer functions. While studying them individually may be helpful, it will not demonstrate when one noise contribution exceeds another. The contributions are expressed on a common output-referred basis and the ratio between the Leeson frequency f_L and the loop bandwidth F_{BW} can be directly evaluated in the composite model.

Let $G(s) = \frac{K_{PD}K_{VCO}Z(s)}{s}$ denote the open-loop gain, with $Z(s)$ the loop filter impedance and K_{PD}, K_{VCO} the phase-detector and VCO gains, respectively. The closed loop response between the PFD input (where the reference (DDS) noise source and the phase detector and divider noise source are injected) and the VCO output is [6]:

$$CL(s) = \frac{G(s)}{1 + G(s)/N}, \tag{2}$$

while the response from the VCO itself to the output is [6] :

$$T_{VCO}(s) = \frac{1}{1 + G(s)/N}. \tag{3}$$

All the noise sources are mutually independent, so their powers spectral densities sum at the PLL output [6]. The internal PLL-chip noise (PFD/CP flat and flicker components) is injected at the same node as the DDS reference and is thus shaped in the same way by $CL(s)$; it is therefore absorbed into the term $S_{\phi,PFD/CP}(f)$, which is already present in Eq. (4) of the reference-path. The noise, on the other hand, is injected directly at the VCO tuning node: it is first transformed into an equivalent phase contribution by the VCO gain. It is then multiplied by the same high pass function $T_{VCO}(s)$ that governs the free-running VCO noise, because the loop is unable to tell the difference between it and

$\left|\frac{K_0}{j2\pi f}\right|^2$ at that node. The output phase noise spectrum of the single sideband is thus:

$$\begin{gathered} S_{\phi,out}(f) = |CL\,(j2\pi f)|^2 . \\ \left[S_{\phi,DDS}(f) + S_{\phi,PFD/CP}(f)\right] \\ +|T_{VCO}(j2\pi f)|^2 . \\ \left[S_{\phi,VCO}(f) + \left|\frac{K_{VCO}}{j2\pi f}\right|^2 . S_{V,filter}(f)\right] \end{gathered} \quad (4)$$

For offset frequencies $f \ll F_{BW}$, the loop gain satisfies $|G(j2\pi f)/N| \gg 1$, so $CL(j2\pi f) \to N$ and $T_{VCO(j2\pi f)} \to 0$. The reference-side noise is therefore transferred to the output scaled by N² in power, while the intrinsic VCO phase noise is suppressed. For $f \gg F_{BW}$, however, $CL(j2\pi f) \to 0$ and $T_{VCO(j2\pi f)} \to 1$, so the output phase-noise spectrum approaches the sum of the free-running VCO noise and the loop-filter noise $S_{V,filter}(f)$. For the case considered here, the VCO term $S_{\varphi,VCO}(f)$ in Eq. (4) is the Type 1 Leeson spectrum from Section II, whose $1/f^3$, $1/f^2$ and white-noise asymptotes are separated by the amplifier flicker corner f_c and the Leeson frequency f_L given in Eq. (1). The reference-path term includes $S_{\varphi,DDS}(f)$ from the DDS model in [2]. After shaping by $|CL(j2\pi f)|^2$, it is combined with the equivalent input-referred flat and flicker PFD/CP terms on the same output-referred scale.

To describe the relative placement of the Leeson transition and the PLL bandwidth by a single dimensionless parameter, define

$$k \equiv \frac{f_L}{F_{BW}} . \quad (5)$$

The ratio is defined as Eq. (5) rather than its inverse. With this choice, $k \gg 1$ corresponds to the intuitive VCO-dominated case, with the Leeson transition far above the loop bandwidth, and $k \ll 1$ to a reference-dominated spectrum. The definition thus matches the physical regimes described below instead of requiring an inverted reading.

Three qualitative regimes of k characterize the relative placement of the Leeson transition and the PLL loop bandwidth:

- $k \gg 1$ (f_L far above F_{BW}): the Leeson transition lies well above the loop bandwidth, where $T_{VCO}(j2\pi f)$ approaches unity. A substantial portion of the free-running VCO $1/f^2$ noise region then remains outside the loop's suppression range, and the VCO contribution is likely significant over a broad offset range.
- $k \ll 1$ (f_L far below F_{BW}): the loop suppresses the intrinsic VCO noise through the Leeson transition and into the white-noise region, increasing the relative weight of the reference path within the loop bandwidth.
- $k \approx 1$: the Leeson transition and the loop-bandwidth region overlap, so the loop shifts from suppressing to passing the intrinsic VCO noise near the transition, producing a pronounced VCO-vs-reference trade-off.

For all three regimes, k indicates which noise source is able to dominate the spectrum. It does not tell us which source actually does, because that also depends on the absolute noise levels of the reference/PFD-CP path and the VCO. This means that $k \approx 1$ is not an optimum in general, and the bandwidth that minimizes the integrated phase noise still has to be determined from the complete composite spectrum of Eq. (4) over the offset range of interest.

The benefit of k over the classical BW_{JIT} crossing-point construction is that it requires very little information. The fully output-referred reference/PFD-CP curve is needed to find BW_{JIT}, and the loop transfer functions, K_{PD}, K_{VCO} and N are needed to obtain that curve. To evaluate k, on the other hand, a qualitative comparison of the reference-and-PLL-chip path with the VCO is sufficient, provided the VCO has been characterized. Thus, k can be used before the reference and PLL-chip parts are finalized.

Equations (4) and (5) will be used in the

following sections to compare measured phase-noise spectra with model predictions.

VI. Simulation Methodology and Model Verification

To give a first quantitative evaluation of the k trade-off before the next iteration of the hardware, eq. (4) was numerically solved with DDS, VCO and PLL parameters that were chosen for the experimental setup. The reference path follows [2] where a signal is generated by the AD9913 DDS clocked by a CCHD-575X-25-125.000 reference oscillator, and directly fed to the PFD (R = 1, N = 3, $f_{PFD} = 16MHz$). The VCO is characterized at near $f_0 \approx 48\,MHz$, where $Q_L = 12$, $Q_I \approx 35$ for this evaluation, and $f_c \approx 600Hz$. The data from the datasheet and the free-running measurements taken with a PN2060C phase-noise analyzer are used to estimate $f_L \approx 2MHz$ from Eq. (1).

According to ADIsimPLL [8], these are the normalized ADF4001 PFD/CP noise coefficients: $PN_{1kHz} = -214\,dBc/Hz$ and $PN_{10kHz} = -117\,dBc/Hz$. The loop filter is a third-order passive circuit, designed with the time-constant method of [6] with a desired phase margin of 80° (γ = 1, T_{31} = 0.6). Resistor thermal noise enters Eq. (4) through $|T_{VCO}|^2$. The first candidate bandwidth, F_{BW}, is obtained by finding the intersection of the free running VCO curve and the combined reference/PFD-CP curve [6]. This intersection is at $F_{BW} = 556.6kHz$ which results in the first candidate value of $k = 3.59$ (Fig. 2) for the present parameter set.

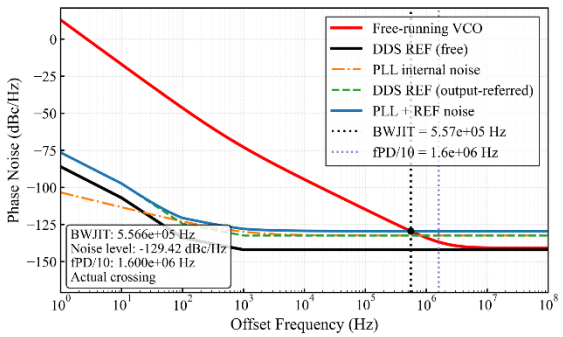


Fig. 2. *Defining candidate F_{BW}*

At this operating point, an integration over $12kHz - 20MHz$ results in an RMS phase error of 0.05° and RMS jitter of 2.8988 ps. For F_{BW} and the other filter parameters fixed, one sweep is to change Q_L; another sweep can be to change F_{BW} with Q_L fixed. This is the range of k which is used in the next section to separate resonator and loop effects.

VII. Results and Discussion

Fig. 3 shows the individual noise contributions that are broken down at the candidate operating point determined in Section VI:

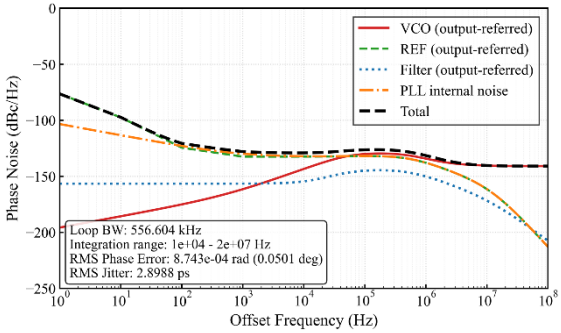


Fig. 3. *Output PN contributions*

At this operating point, the DDS-referenced and PFD/CP contributions dominate below F_{BW}, while the free-running VCO and loop-filter noise dominate above it, consistent with the qualitative picture developed in Section V. Sweeping Q_L from 1 to 30 at fixed F_{BW} spans k from approximately 43 down to 1.4, directly exercising the three regimes identified in Eq. (5); the resulting evolution of the full output spectrum is shown in Fig. 4:

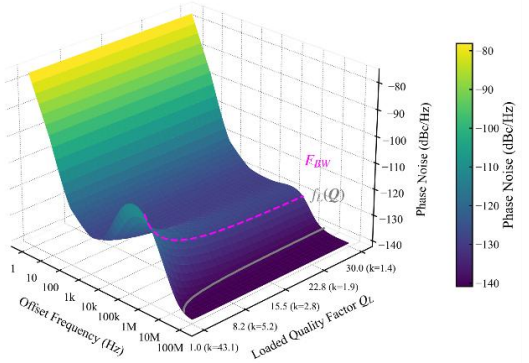


Fig. 4. *Output Phase Noise vs Q_L*

At low Q_L (large k), the Leeson transition lies far above F_{BW} and the free-running VCO noise remains visible over a wide offset range, consistent with the $k \gg 1$ regime; as Q_L increases and k approaches unity, the transition shifts into the loop-suppressed region and the spectrum flattens toward the reference/PFD-dominated floor. The corresponding integrated metrics are summarized in Fig. 5:

The RMS phase error/jitter and the phase noise at 1 kHz offset monotonically decrease with increasing Q_L (decreasing k); however, the rates of decrease are quite small for $Q_L \approx 5-15$ $(k \approx 8.4-2.9)$. Further Q_L improvement beyond this point gives little benefit as the reference/PFD-chip floor is the limiting factor.

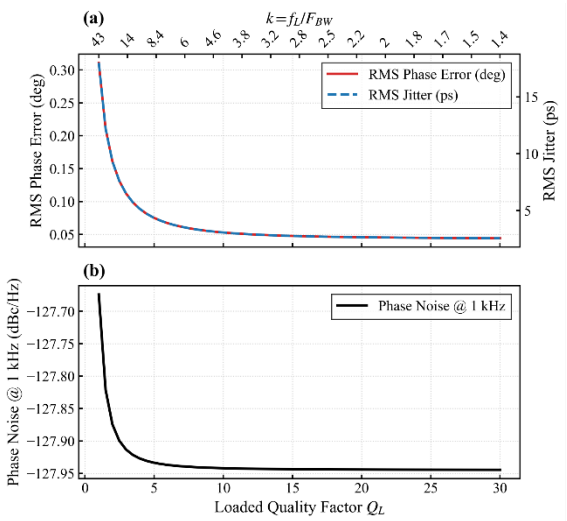


Fig. 5. *RMS phase error (PE), Jitter and PN@1k vs k and Q_L*

Instead of changing the resonator $Q_L = 12$ $(f_L = 2MHz)$ is fixed and the loop is swept. Fig. 6 reveals a clear minimum in RMS jitter at $F_{BW} = 542.88kHz$, $k = 3.684$ which is close to, but not exactly equal to the BW_{JIT} crossing estimated in Section VI. This validates the cautionary note given in Section V: the crossing frequency is a good first guess for the jitter optimal bandwidth, but the actual jitter optimal bandwidth, as gained from the full integrated composite spectrum here, is slightly different, in line with the non-ideal (non-brick-wall) roll-off of the realized loop filter. The phase noise at 1 kHz in the same figure does not share this minimum: it keeps improving monotonically with narrower bandwidth. This shows that no single value of F_{BW}, or equivalently of k, is optimal for all performance metrics, in agreement with the qualitative discussion in Section V.

To be more general than the single measured operating point above, the same composite framework is used for a wider range of reference and PLL-chip path scenarios, because in practice the designer will only know the VCO characteristic, with reference and PLL-chip path noise specified by parts that are not yet selected or characterized.

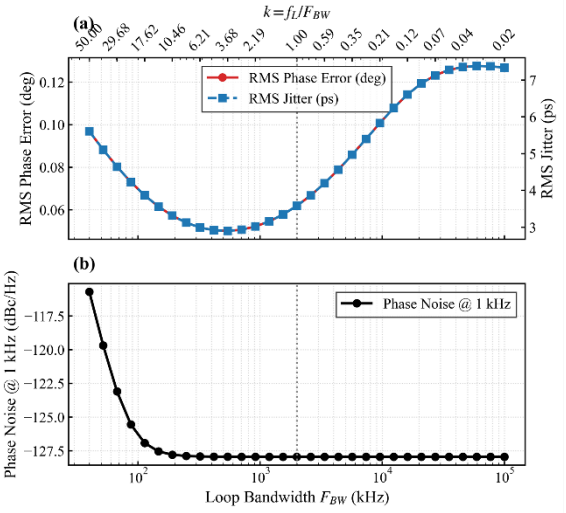


Fig.6. *RMS PE, Jitter and PN@1k vs k and F_{BW}*

The seven cases considered are: comparable, moderately better, moderately worse, substantially better, and substantially worse than the VCO, for the REF/PLL path as a whole. Two other cases are considered in which a substantially better reference combined with a PLL-chip comparable to the VCO, and conversely a substantially better PLL chip combined with a reference comparable to the VCO.

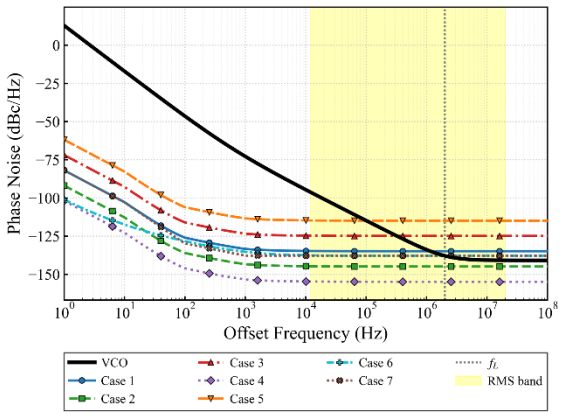


Fig.7. *REF/PLL PN levels relative to the VCO*

In each scenario, F_{BW} is swept to find the jitter-minimizing bandwidth and the associated k, and thus the VCO dominated, transition, and reference dominated regimes of Eq. (5) are studied systematically, rather than for a fixed hardware configuration. Across the seven scenarios, the jitter-optimal k ranges from $k \approx 0.37$ to $k \approx 21$ (Table I), populating all three regimes defined in Section V.

Cases 3 and 5, where the reference/PLL-chip path is noisier than the VCO, occupy the $k \gg 1$ regime, leaving the Leeson transition largely unsuppressed. Cases 2 and 4, with a favorable reference/PLL path, fall into $k \ll 1$, placing the transition well inside the suppressed region.

Table I. *Optimal F_{BW}, jitter and k per scenario*

Case	F_{BW}	*RMS jitter*	$k \equiv \frac{f_L}{F_{BW}}$
1	1.016MHz	2.511ps	1.97
2	5.33MHz	1.915ps	0.37
3	310.5kHz	3.404ps	6.44
4	5.33MHz	1.770ps	0.37
5	95.3kHz	5.260ps	20.99
6	1.75MHz	2.349ps	1.14
7	1.75MHz	2.349ps	1.14

Cases 1, 6, and 7 lie near $k \approx 1$ and show the anticipated VCO–reference trade-off. However, Cases 6 and 7 converge because the "comparable" component dominates the REF/PLL power sum, whereas the substantially better component is negligible. Thus, $k \approx 1$ does not itself define the jitter optimum, which must be obtained from the full composite spectrum of Eq. (4).

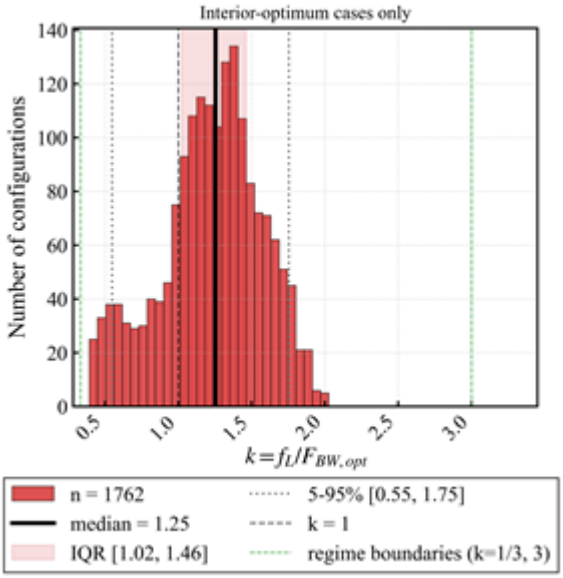


Fig.8. *Summary interior histogram*

To assess whether the near-unity k observed in Cases 1, 6, and 7 extends beyond a single parameter set, a Monte Carlo study was performed over the REF-better/PLL-comparable-to-better design space. The measured VCO parameters and $N = 3$ were fixed, while REF/PLL noise and loop-filter parameters were randomized across 3500 draws spanning seven REF types. At each draw, F_{BW} was optimized for minimum RMS jitter under $F_{BW} \leq f_{PFD}/3$. For the entire set of 3500 draws, the median k was 0.42.

Of these, 1738 configurations (49.7%) reached the imposed bandwidth limit. For the remaining 1762 configurations with a genuine interior jitter minimum, the median k was 1.25 and the $5-95\%$ range was 0.55–1.75 (Fig. 8).

CONCLUSION

The ratio $k = f_L/F_{BW}$ is a measure of how the VCO Leeson transition and PLL bandwidth are placed relative to each other, and is not a measure of the jitter optimum per se without the consideration of the entire composite spectrum. Of the 3500 configurations in the Monte Carlo study, 1738 (49.7%) reached the imposed bandwidth limit. If a true interior minimum was present, the optimum k was clustered around unity, with a median of 1.25, and a 5-

95% range of 0.55-1.75 for the REF types examined. Thus, $k \approx 1$ represents a practical trade-off region under the assumed design space, not a universal optimum. The numerical optimum and the boundary-limited behavior still need to be validated by closed loop hardware measurements.

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