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ENHANCING THE MEASUREMENT OF BIO-FET TRANSISTOR PARAMETERS WITH DIGITAL ELECTRONICS

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Abstract

Accurate characterization of Bio-FET and OECT devices requires control of the applied voltages together with current measurement over a wide range, because the measuring circuit itself may change the transistor operating point. The considered system uses an STM32 controller, galvanic isolation, an ADS1220 24-bit delta-sigma converter and several current ranges; the high-current path is based on an INA240 amplifier and Kelvin shunt, while the lower-current part is assigned to more sensitive shunts or a transimpedance stage. The required interval is 1 microampere to 1 ampere and cannot be covered well by one fixed shunt, so automatic range selection is included. Firmware performs filtering, calibration and shunt-drop correction, and the same chain is intended for transfer/output sweeps, gate-current recording, transconductance calculation and stability tests. Final uncertainty remains an experimental result of the implemented hardware.

Keywords: *Bio-FET, OECT, digital measurement, current sensing, ADS1220, INA240, galvanic isolation, STM32, automatic ranging.*

INTRODUCTION

Bio-FET devices convert changes at a biological or electrochemical interface into an electrical response, and in OECTs ions from the electrolyte modulate the bulk conductivity of the organic semiconductor channel, which can provide high transconductance at relatively low operating voltage [1]. The gate-electrolyte and channel-electrolyte interfaces are part of the sensing process [2], while the mixed ionic-electronic conductor strongly affects transistor behavior [6]. In the present case the platform records I_D, V_DS, V_GS, I_G, time and temperature, allowing both electrical characteristics and slower drift to be followed from the same measurement sequence.

OECT characterization may use source-measure units, potentiostats and combined current/voltage instruments, while two-channel AC potentiostat measurements have also been applied to conductance, transconductance, conductivity, volumetric capacitance and mobility-related quantities [5]. The aim here is not to replace these instruments, but to organize the analog front end, isolation, conversion, calibration and firmware in one repeatable digital chain which can later be compared with reference equipment. Such hardware is useful when many Bio-FET/OECT sweeps have to be repeated under the same conditions [2], [10].

The investigated current interval is 1 microampere to 1 ampere, or six decades, and is adopted as an engineering requirement of the instrument rather than taken from the literature. One fixed shunt gives a direct compromise: a large resistance improves the signal at low current but increases burden voltage at high current, whereas a small resistance behaves better

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near the ampere range and gives almost no useful voltage near 1 microampere. The current path is therefore divided into several ranges, with ADS1220 providing programmable gain, differential inputs, digital filtering and temperature sensing [3].

The architecture is considered together with the measurement procedure, because the circuit diagram alone does not define useful accuracy. The main requirements are galvanic separation from the host computer, current acquisition over 1 microampere to 1 ampere, measurement or correction of V_DS and V_GS, range-specific calibration and automatic extraction of Bio-FET/OECT parameters. The nominal 24-bit ADC word is not treated as 24-bit system accuracy; offset, leakage, component tolerance, switching and temperature effects are left for experimental evaluation.

DIGITAL MEASUREMENT SYSTEM

Figure 1 shows the measurement architecture. The STM32 communicates with the PC through USB and controls sequencing, range selection, acquisition, calibration and data transfer, while the analog domain is supplied through an isolated DC/DC stage and the SPI link to ADS1220 crosses a digital isolation barrier. Thus the USB/PC ground is separated from the local Bio-FET reference; the actual influence of this arrangement on common-mode behavior and noise will be checked on the complete hardware.

ADS1220 is used as the precision conversion stage and provides 24-bit delta-sigma conversion, data rates up to 2 kSPS, PGA gains from 1 to 128, differential or single-ended inputs, SPI communication, internal reference and an on-chip temperature sensor [3]. In the present system it works together with the analog ranges, not instead of them. The internal sensor is recorded as board/ADC temperature; if shunt self-heating becomes significant, a separate sensor near the shunt can be added.

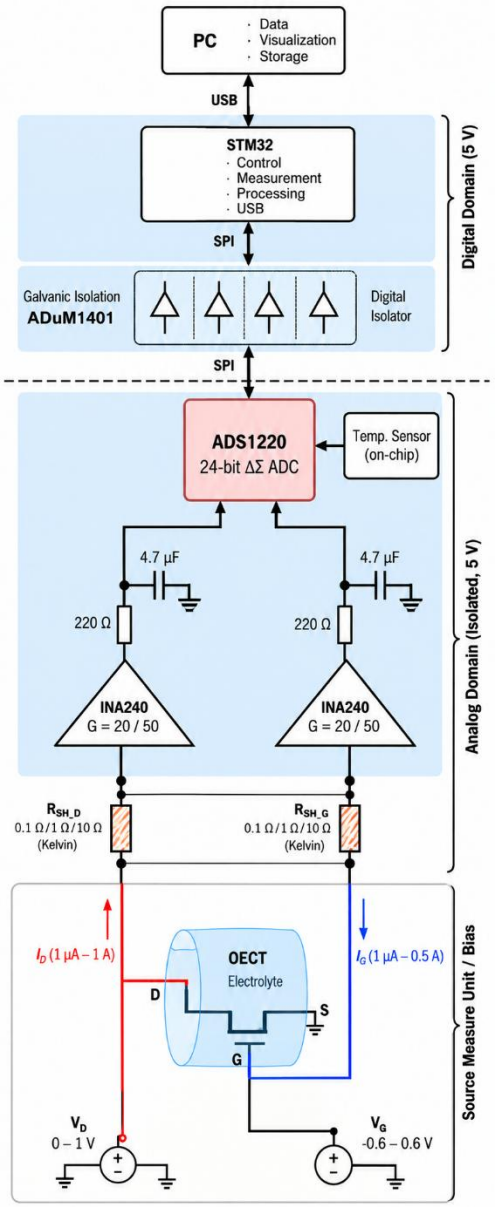


Fig. 1. *Principle measurement schematic for Bio-FET/OECT* drain *and gate currents (I_D and I_G).*

CURRENT MEASUREMENT AND RANGE SELECTION

For the high-current drain range, I_D is obtained from the voltage across a precision Kelvin-connected shunt. With shunt resistance R_SH and current-sense gain G, the amplifier output is

$$V_OUT = V_REF + G \cdot I_D \cdot R_SH$$

For unidirectional operation with V_REF close to zero, the current estimate becomes

$$I_D = V_OUT / (G \cdot R_SH).$$

For the highest drain-current range the calculation uses R_SH = 0.1 ohm and INA240A1 with G = 20 V/V. This gives 0.1 V shunt drop and 2.0 V ideal amplifier output at I_D = 1 A; at 100 mA the corresponding values are 0.01 V and 0.2 V. These are circuit calculations, not measured data. INA240 operates from 2.7 to 5.5 V, supports -4 V to 80 V common mode and fixed gains of 20, 50, 100 and 200 V/V [4], while ADS1220 accepts 2.3 to 5.5 V supplies [3], so an isolated 5 V domain is compatible with both devices.

For the gate-current path, where the design limit is 0.5 A, R_SH = 0.1 ohm and INA240A2 at G = 50 V/V give 2.5 V full-scale output and 50 mV shunt drop. The same path cannot resolve 1 microampere: the shunt voltage is only 0.1 microvolt before amplification, while INA240 has a specified maximum input offset of 25 microvolts [4]. Separate sensitivity ranges are therefore required; ADC bit depth alone cannot cover the complete interval.

The range partition contains the 0.1-ohm/INA240 branch for the highest current, a higher-sensitivity current-sense branch in the middle region and a dedicated transimpedance/electrometer stage near the microampere limit. Exact switching thresholds, feedback resistance and switch topology remain for experimental selection. Adjacent ranges are intended to overlap and the firmware uses hysteresis so that a current close to one boundary does not cause repeated switching.

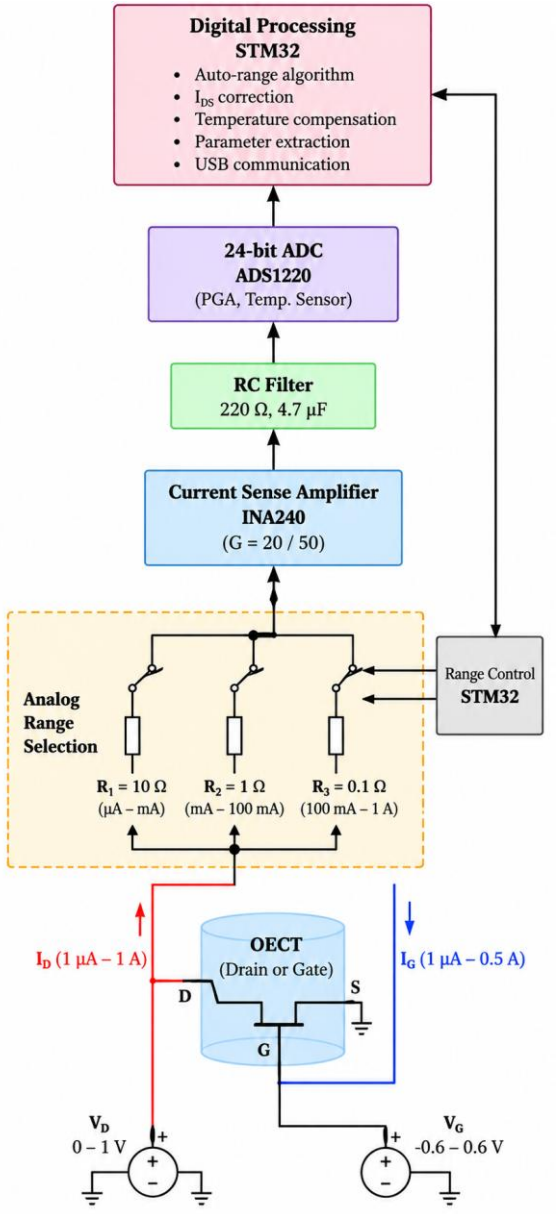


Fig. 2. *Auto-range current-measurement architecture covering 1 microampere to 1 ampere.*

VOLTAGE-DROP CORRECTION AND FILTERING

A shunt introduces burden voltage and changes the voltage actually applied to the transistor. When it is connected in series with the drain supply, the real device voltage is

$V_{DS,real} = V_{DS,set} - V_{SH} = V_{DS,set} - I_D \cdot R_{SH}$.

With R_SH = 0.1 ohm, V_SH reaches 0.1 V at I_D = 1 A.

This is 2% of a 5 V drain setting and about 0.67% of a 15 V setting, which shows when the correction becomes relevant. Firmware can estimate V_DS,real from measured current and calibrated R_SH, while direct differential sensing of drain and source remains the preferred validation method when the actual transistor voltage is required.

The proposed analog output filter uses R = 220 ohm and C = 4.7 microfarad, giving an ideal first-order cutoff near 154 Hz from f_c = 1/(2*pi*R*C). This is only the external RC

value because ADS1220 digital filtering, output data rate and settling also affect the effective bandwidth [3], [8]. Final acquisition rate, delay after switching and firmware averaging will therefore be selected from measured noise and settling data.

DIGITAL PROCESSING AND PARAMETER EXTRACTION

Firmware stores calibration coefficients separately for every range, including shunt or feedback resistance, analog gain, zero-current offset, ADC scale factor and temperature coefficients where measurements justify them. Zero-current readings can be made at start-up or between measurement sequences, while samples immediately after a range change are rejected until the analog path and ADC settle. Range switching uses hysteresis. These functions form part of the proposed protocol and require implementation-level validation.

For every operating point the record contains V_DS, V_GS, I_D, I_G, temperature, active range, timestamp and validity flags, which allows later reconstruction of the exact measurement condition. From a transfer characteristic I_D(V_GS) at fixed V_DS, transconductance is evaluated numerically as

$$g_m = dI_D / dV_GS.$$

Output characteristics are obtained from I_D(V_DS) at selected gate voltages, while transconductance is derived from the transfer curve; both are standard transistor descriptors [9]. OECT measurements may additionally include conductance, mobility-related parameters and volumetric capacitance [5], [6], but these are not inferred from the DC data here. I_G is stored as an independent channel because gate behavior may be relevant to the electrochemical interface.

The digital workflow includes automatic sweeps, defined dwell times, forward and reverse scans, long-duration logging and synchronized metadata. Reverse sweeps can be used to examine hysteresis, while constant-bias records are suitable for drift measurements. The effect of timing and filtering on repeatability will be checked first with reference loads and then with Bio-FET/OECT devices.

ERROR BUDGET AND EXPECTED PERFORMANCE

The nominal 24-bit ADC word must not be interpreted as 24-bit accuracy of the complete instrument. Texas Instruments specifies up to 20 effective bits for ADS1220 under stated conditions [3], and precision-ADC guidance separates nominal resolution from total system error [7]. The present error budget also includes shunt tolerance and temperature coefficient, amplifier offset and gain error, thermal EMFs, PCB leakage, switching resistance and calibration uncertainty. The INA240 maximum input offset of 25 microvolts and maximum gain error of 0.2% [4] are especially important near the lower limit of a shunt range.

Validation will be carried out separately for every current range using a calibrated current source, source-measure unit or traceable voltage/resistance combination. After settling, repeated samples will provide mean error, standard deviation and relative error together with temperature, and extra points near range boundaries will show whether offset, gain or shunt mismatch produces a visible discontinuity. No numerical uncertainty is assigned before these measurements are completed.

The planned validation points are 1 microampere, 10 microampere, 1 mA, 100 mA, 0.5 A and 1 A, with additional points around range transitions. For each point the reference value, measured mean, relative error, standard deviation, temperature and active range will be recorded. These are proposed test points; experimental values remain TBD until the PCB is assembled and calibrated.

Figure 3 summarizes the calculated current-resolution ranges and proposed operating regions, not experimental accuracy.

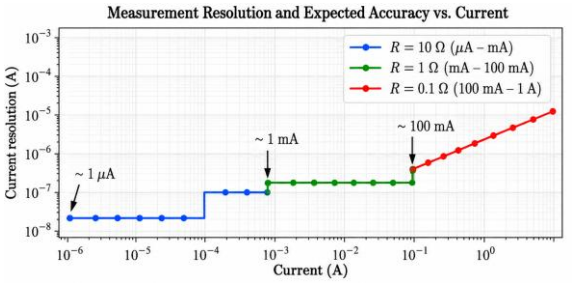


Fig. 3. *Theoretical current-resolution ranges and summary of the measurement parameters.*

Hardware tests will compare raw and calibrated data, quantify noise and temperature dependence and verify continuity across automatic range changes. This distinction is kept so that calculated resolution is not mixed with uncertainty which can only be obtained by measurement.

Table 1. Measurement ranges, resolution and expected accuracy (theoretical).

Range	Shunt resistor R_{SH}	INA240 gain (G)	Current range	ADC input range (typ.)	Current resolution (LSB)	Expected accuracy (typ.)
Range 1 (μA – 1 mA)	10 Ω	50	1 μA – 1 mA	0 – 0.5 V	≈ 1 μA	±(0.5 – 1)%
Range 2 (mA – 100 mA)	1 Ω	50	1 mA – 100 mA	0 – 2.5 V	≈ 1.5 μA	±(0.2 – 0.5)%
Range 3 (100 mA – 1 A)	0.1 Ω	20	100 mA – 1 A	0 – 2 V	≈ 7.5 μA	±(0.2 – 0.5)%

Note: Resolution is calculated for ADS1220 with 24-bit nominal resolution (≈ 20 effective bits) and 2.5 V reference.

EXPERIMENTAL MEASUREMENT PROTOCOL

The experimental protocol is based on repeatable bias sweeps. Before a device measurement, an electronic zero is recorded for the active ranges together with board temperature; after connection, V_DS and V_GS are applied only after range and compliance limits are configured. Each bias point is stored after a defined settling interval together with standard deviation, active range, temperature and timestamp. The final settling time will be selected from the measured analog and digital response [3], [8].

For a transfer characteristic, V_DS is held constant while V_GS is stepped and both I_D and I_G are recorded; a reverse sweep with the same dwell time can be used to observe hysteresis. For output characteristics, V_GS is fixed while V_DS is swept, and transconductance is then obtained from the transfer data. Additional OECT transport and frequency-domain quantities described in [5], [6] can be added later without changing the basic acquisition procedure.

The complete current span will also be verified without a transistor, using calibrated electrical references so that instrument error is not mixed with device behavior. The planned points from 1 microampere to 1 A are measured after zero correction, with additional values around every range boundary; overlap data are used for gain/offset correction and for checking continuity. These steps define the validation procedure and are not completed measurements.

Noise is evaluated with a constant input and one fixed range, using time-domain records for peak-to-peak variation and standard deviation, while repeated measurements at several ADS1220 data rates show the bandwidth/resolution trade-off [7], [8]. The same input will be kept during these tests so that changes caused by automatic ranging are not mixed with converter noise. Temperature drift is checked after thermal stabilization and, where possible, at several ambient temperatures, allowing converter noise, amplifier offset and shunt drift to be examined separately before a combined uncertainty budget is prepared. This part of the validation is particularly important for longer Bio-FET measurements, where slow electronic drift could otherwise be confused with a real change of the device.

A regulated isolated 5 V domain is within the specified supply range of both ADS1220 and INA240 [3], [4]. With the proposed 0.1-ohm shunt and gain 20, the drain path maps 0.1-1 A to approximately 0.2-2.0 V, while the gain-50 gate path gives about 2.5 V at 0.5 A. These values are calculated design points and are used mainly to check that the expected signals remain inside the useful converter range. Real output swing, ADC limits, tolerances, temperature rise and transient behavior still have to be checked on the final PCB, especially close to the upper

range limits where shunt dissipation becomes larger.

The design analysis shows why ADC bit depth alone cannot define performance over six decades of current. At low current the limiting effects are likely to be offset, leakage, thermal EMFs and noise, while at high current burden voltage, shunt dissipation, interconnection resistance and temperature drift become more important. Kelvin sensing is therefore used for the power shunts and guarded, low-leakage layout will be required around the microampere front end. The two regions have different practical problems and should not be described with one resolution figure. Their actual contribution to uncertainty will be measured for every active range and then compared at the overlap points.

The ADS1220 includes an internal temperature sensor with 0.5 degC typical accuracy according to the manufacturer [3]. Here it is used as a board/ADC temperature indicator, not as direct measurement of the shunt temperature. If high-current operation produces significant self-heating, a separate sensor can be placed close to the resistor and its temperature correlated with the measured current error before any correction is introduced. In this way a temperature coefficient, if finally used in firmware, will be based on an observed relation in the assembled measurement channel and not only on the component datasheet.

Galvanic isolation separates the USB/PC ground from the local analog reference of the Bio-FET circuit and is intended to reduce unwanted ground-current paths when other laboratory equipment is connected. It does not remove the need for a defined analog reference and proper shielding, and it also does not guarantee lower noise by itself. Its actual influence on common-mode behavior, leakage and measurement noise will therefore be included in the experimental evaluation, using the same wiring conditions that will later be applied during transistor measurements.

CONCLUSION

A digitally controlled architecture for Bio-FET/OECT parameter measurement is presented, combining STM32 control, galvanic isolation, ADS1220 conversion, range-dependent current sensing, digital processing and temperature logging. The adopted interval from 1 microampere to 1 ampere is an engineering requirement and is divided into overlapping analog ranges because different error sources dominate at the two ends of the span. Circuit calculations define the expected shunt drops, amplifier outputs, filter cutoff and operating regions, while the measurement protocol defines how zero correction, range changes, dwell time and reference comparison will be applied. At this stage these calculations establish the structure of the instrument; noise, drift, uncertainty and range-transition continuity remain quantities for hardware calibration.

For the high-current drain range the selected design uses a 0.1-ohm Kelvin shunt with INA240A1 at G = 20 V/V, while the gate path up to 0.5 A uses INA240A2 at G = 50 V/V; the relevant device specifications are taken from [3], [4]. The next stage is implementation and calibration of the complete PCB against traceable electrical references, first without a transistor and afterwards with Bio-FET/OECT devices. The planned device tests include transfer and output characteristics, independent I_G recording, numerical transconductance, short-term noise, longer drift, temperature effects and the behavior at automatic range transitions. The results from these measurements will determine which ranges and correction coefficients are retained in the final instrument.

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